Reliability Enhancement of Industrial Capacitor Banks through Smooth Engagement to the Grid

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Abstract - Most of the industries with inductive loads, results in a lower power factor due to the lagging power factor quality of inductive loads. In order to maintain a better power factor, capacitor banks are used in industry. Due to the leading power factor quality of capacitors, capacitor banks neutralize the effect of inductive loads to improve the power factor. However, these capacitor banks are having less lifetime. This is due to adverse effects of transient voltages and currents mainly owing to capacitor bank Energization and switching. Existing methods of grid engagement; the switch or connector module which connects capacitor banks to the grid, can be considered as a main reason for this. In this study the behavior of transients in the capacitor banks and power system was analyzed using MATLAB Simulink and a better switching mechanism was introduced. By advancing the existing Pre-Insertion Resistor capacitor banks protective mechanism, the Pre-Insertion Resistor Intermediate Step (PIRIS) mechanism was developed. An Intermediate resistive path has been introduced for the Pre-Insertion resistor mechanism in order to further mitigate the switching transients. Switching times and resistor values were optimized using simulations.

Keywords: Capacitor banks, Condition monitoring, Pre -insertion resistors, Transients, Power factor

I. INTRODUCTION

Power factor is the ratio of working power to apparent power used in a power network. It also can be defined as the power efficiency. To counterbalance the adverse effects of inductive loads, capacitor banks are used as they possess leading power factor quality[1]. Improvement of the power factor maintains the quality of the power system; by avoiding any blackouts due to excess demand of power, increases energy efficiency and reduces electricity costs, and reduces failure of electric instruments[2].

However, the reliability of capacitor banks which are used for the power factor improvement is a problem, because failures of capacitors are more frequent in the industry. There are considerable occurrences which affect the lifetime of the capacitor banks and quality of the power system due to generation of high voltage and current transients originating from various artificial and natural occurrences [2,3].

As an industrial practical solution, introduction of smooth capacitor banks switching mechanism mainly for the mitigation of voltage transients due to switching of capacitor banks was concerned in this study. More Importantly, cost effectiveness and simplicity of the protective mechanism were prioritized when considering the practical constraints in developing countries like Sri Lankan industry.

II. METHODOLOGY

A thorough literature reviews mainly based on the research papers was done to get a broad idea about disturbances from capacitor banks to the power system and effects to the capacitor banks from the grid.

In order to get a better understanding about practical conditions, using the information of an industrial application (WTC, 36 stories building) model of this existing power system was designed in the MATLAB Simulink software. In this study potential solution tests were carried with a MATLAB model. Practically it's challenging to switch capacitor banks on zero voltage points to eliminate inrush current [4,5]. Therefore, intermediate Step Switching Mechanism was developed to mitigate switching/ energization inrush transients in the power system. Pre-insertion resistor intermediate step switching Mechanism is an advancement of the existing pre-Insertion resistor protective mechanism.

Pre-insertion resistor procedure initially uses a higher resistive path for the connection of capacitor banks to the power system, then the high resistive path will be bypassed [4,6]. The basic architecture is shown in figure B. Even though the transients were mitigated when connecting capacitor banks to the grid in the conventional method, noticeable transitions were generated when switching from the resistive path to the direct path.

In PIRIS mechanism switching transitions have been further decreased by introducing an intermediate resistive path with having any effect to the power factor. Figure A shows the basic architecture of the mechanism.

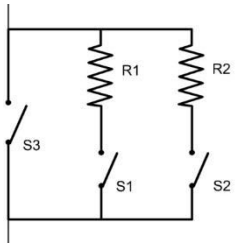

Figure A

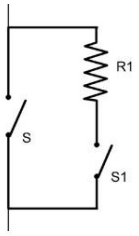

Figure B

When introducing a high resistive path according to V = IR and P = V^2/ R voltage, current transient due to sudden voltage difference can be mitigated. For a short period of time transient energy will be wasted as P= V^2/R.

Based on research publications, a range of switching times were tested to get the optimal values of resistivity for better performance.

III. RESULTS AND DISCUSSION

The pre insertion resistor path was an acceptable solution for the mitigation of transients in the switching process which is already existing. But still, the variation from an infinite resistance value to a particular resistance and then from a high value to null can still create harmful transients. The intermediate step pre insertion was proposed with the idea of smooth engagement of the capacitor bank to the power system.

The MATLAB simulation model of the common area of WTC building Colombo (model used for the solution testing) is mentioned below. Some figures were slightly altered in order to obtain clear wave forms.

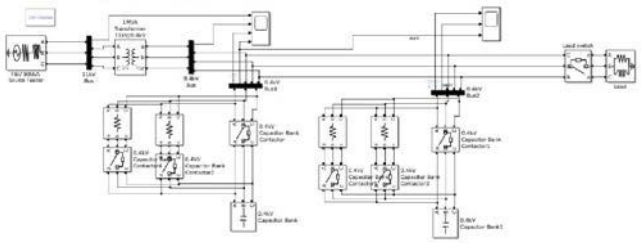

Figure C: MATLAB Simulink model (Ref: WTC common area power system)

Here the capacitor banks energization, back to back switching of capacitor banks were analyzed under conditions of no protective mechanism, with Pre-Insertion resistor protective mechanism and proposed PIRIS protective mechanism. The results obtained from the above scenarios were demonstrated in the below table.

	Capacitor Bank Energization		Capacitor Bank Back to Back switching	
Transient	Current	Voltage	Current	Voltage
Without any protection	497.3 A	671.6 V	1440 A	441 V
With Pre Insertion	385.6 A	337.4 V	434.5 A	360.1 V
With PIRIS mechanism	349.8 A	235 V	367.7 A	358.9 V

Table 1: Results table with and without PIRIS initial stage

Above results demonstrate that 10.23% and 30.34% percentages of current and voltage transients were mitigated when comparing the existing Pre-Insertion resistor mechanism and PIRIS mechanics in the Capacitor Bank Energization scenario. While in the Back to Back switching scenario 18% and 0.33% respectively the current and voltage transients were further mitigated.

Then the optimization of resistive paths was done by testing the range of resistor values (20 - 80 ohms with 5 ohm gaps) in the MATLAB model. From here the optimal resistor value was taken as 40 ohms which mitigated the transient values the most.

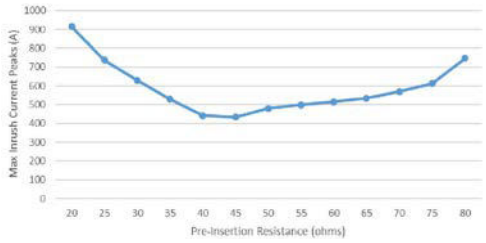

Figure D: Variation of peak inrush current with Pre-insertion resistance

Optimization of switching times of the resistive paths also were done using a range of durations [5] for both Energization and Back to Back capacitor bank switching scenarios. Here, noticeable differences were not analyzed, therefore continued with the 6ms switching period for both resistive paths.

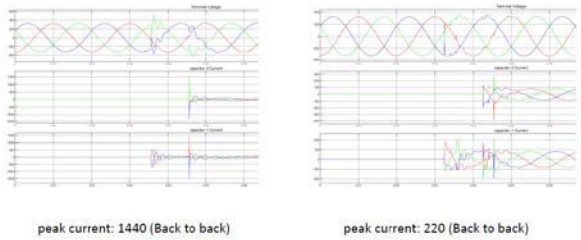

Figure E: Comparison of with and without pre insertion resistance

Finally, a comparison of current waveform graphs, peaks currents of the transients with and without the PIRIS protective mechanism using optimized resistor and resistive paths switching times were demonstrated in figure E.

IV. Conclusion

From the simulations carried out using MATLAB-Simulink and the above evaluations it is clear that a reliability enhancement method was required for a better life expectancy for capacitor banks.

Among the existing protective methods, conventional Pre-Insertion Resistor protective mechanism was simple and effective. Therefore, priority was given for its advancement. In the PIRIS mechanism a new resistive path was introduced to mitigate the capacitor bank switching transients in power systems. When considering the back to back capacitor bank switching scenario current transients were able to suppress up to 18% and in the single capacitor bank energization 10.23% of voltage transients were mitigated compared to the existing Pre-Insertion Resistor method without affecting to the power factor by any means.

With the above demonstrated results it can be concluded that the PIRIS mechanism has a good potential as an Industrial solution. For further studies development of a prototype for this concept and incorporating this mechanism with synchronous switching mechanism can be suggested.

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