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# A TENG Energy Harvesting System with HV Limiting Technique Using Zener Diodes and Impedance Tracking MPPT

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***Abstract*—This document is a Zener diode-limited high voltage (HV) buck converter energy harvesting system for triboelectric nanogenerator (TENG). The TENG commonly generates HV around 100 V. It is impossible to connect directly to switches. However, the proposed system can harvest energy from a wide voltage range of TENG. A long charging time induces wasting energy if it uses a fractional open-circuit voltage (FOCV) to obtain power higher than the breakdown voltage. We propose impedance tracking maximum power point tracking (MPPT), which adjusts the effective impedance of the converter using the pulse-width modulation (PWM) method. We present low-power zero-current sensing (ZCS) based on a common-gate comparator to prevent flowing reverse current from the output stage. The proposed system is designed on a 180-nm bipolar-cmos-dmos (BCD) process. The 40 V Zener-diode array and the highest breakdown voltage of MOSFET in this process are used for utilizing a high voltage input around 100 V. The measured peak conversion efficiency of 89.7 % is achieved for delivering an output power of 1.25 mW.**

***Keywords*—High voltage buck converter, TENG, MPPT, zero-current sensing**

## I. Introduction

With the miniaturization of various electronic devices, portability with convenience has been emphasized [1]. The portability is closely related to the charging and sustaining of power to ensure correct functional operation. Therefore, interest in energy harvesting from ambient has increased. The triboelectric nanogenerator (TENG) [2] is useful for miniaturizing and is suitable for application to the low-frequency motion of the human body. Furthermore, it has a higher energy density than a piezoelectric generator (PEG) [3]. However, the main challenge of TENG as an energy harvesting source is that the TENG usually generates a high voltage (> 100 V) with a high internal impedance (~ MΩ). When the high voltage is applied directly, the inside of the chip can be destroyed. Also, implementing an efficient energy extraction technique is difficult for matching high impedance.

Therefore, this paper proposes a Zener diode-limited high-voltage buck converter to maximize the input power rather than stop the converter operation. The proposed converter uses Zener diodes to extract power and protect the chip. In this 180-nm BCD process, the MOSFETs with a 40 V breakdown voltage cover the high voltage. For 40 V of source input, the converter uses the same power as when it samples 40V for 80 V input voltage without wasting energy with sampling time.

## II. Proposed Architecture

Fig. 1(a) shows the architecture of the proposed diode-limited high-voltage buck converter. It comprises an input source including TENG with a full bridge rectifier (FBR), a 40 V Zener-diode array ($V_Z$), two power switches for buck operation ($M_P$ and $M_N$), and an inductor. A load resistor ($R_L$), an input capacitor ($C_{IN}$), and an inductor ($L$) are off-chip components. The $C_{IN}$ and on-chip FBR offer smooth source voltage of AC voltage from TENG. The 40 V Zener array limits $V_{IN}$ to prevent the breakdown of $M_P$.

Fig. 1(b) shows the block diagram of the system controller, which generates $\Phi_{P,HV}$ and $\Phi_{N,M}$ for $M_P$ and $M_N$, respectively. It consists of a voltage sensing block, an MPPT block, a zero-current sensing (ZCS) block, and two-level shifters (LS). The voltage sensing block tracks $V_{IN}$ and produces low voltage ($V_{sen}$). Using $V_{mpp}$ and $V_{sen}$, the MPPT block generates $\Phi_{P,LV}$. The ZCS block generates $\Phi_N$ based on *c* for controlling $M_N$. Two level shifters use different supply voltages: Low-LS makes $\Phi_{P,LV}$ increases from $V_{DD}$ to $V_m$, and High-LS increases the output of Low-LS from $V_m$ to $V_{IN}$. $V_{DD}$ (=1.8 V) is for logic gates in MPPT and ZCS, $V_m$ (=5 V) is for middle voltage, and $V_{IN}$ is for keeping off-state of $M_P$.

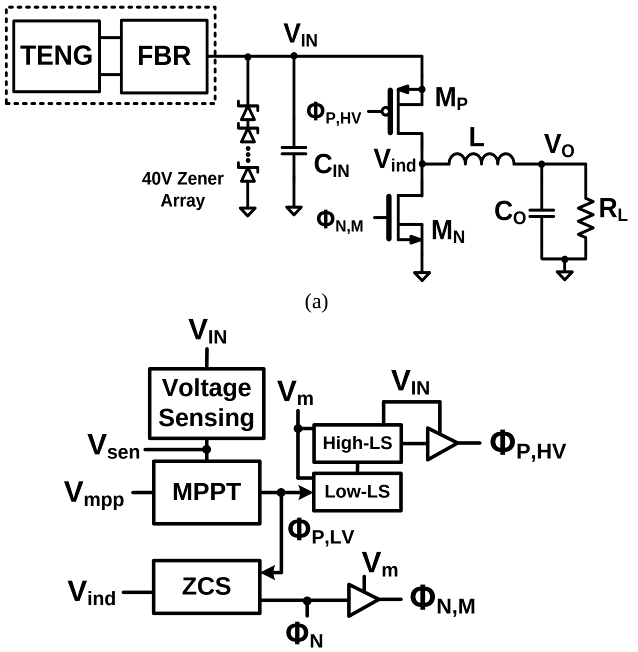


Fig. 1. (a) Architecture of the proposed system, (b) block diagram of the system controller.

Fig. 2 illustrates the operation of the proposed converter ($V_{S/2} > V_Z$). In this case, the average input power ($P_{IN,avg}$) of the converter can be derived as,

$$P_{IN,avg} = \frac{V_Z\left(V_Z - V_O\right)}{2L} \cdot f_S \cdot t_{ON}^2 \cdot \tag{1}$$

Where $L$ is the inductance, $f_S$ is the switching frequency of the converter, and $t_{ON}$ is the on-time of $M_P$. It keeps tracking the maximum power point even though it is impossible to get the exact maximum point ($V_{mpp}$). The effective input impedance ($R_{IN}$) can be derived as follows [4],

$$R_{IN} = \frac{2L}{t_{ON}^2 f_S \left(1-\beta\right)}, \tag{2}$$

where $\beta = V_O/V_{IN}$. Eq. (2) means that the MPPT controller increases the $t_{ON}$ to decrease the effective input impedance of the converter. Fig. 3 shows the calculated result of $P_{IN,avg}$ as a function of $t_{ON}$ when $P_{IN,max}$ = 500 µW with 100V source voltage. Therefore, the proposed system extends the available power range of TENG.

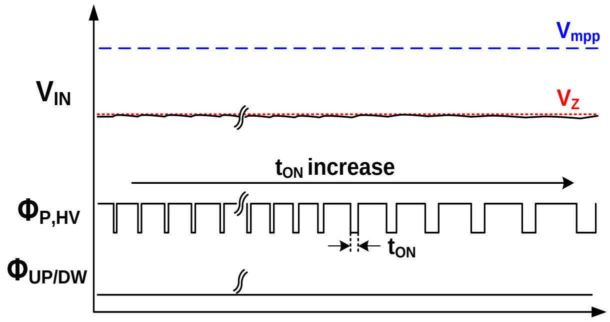

Fig. 2. Operational waveform of the proposed converter. ($V_S/2 = V_{mpp} > V_Z$)

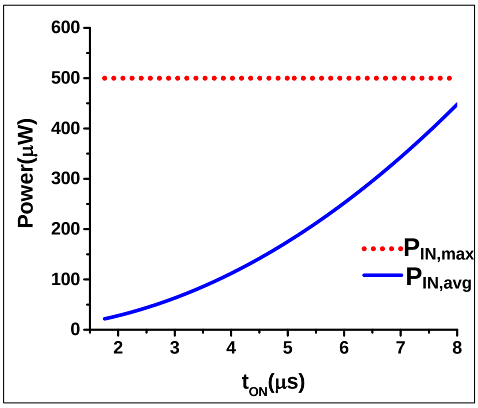

Fig. 3. The calculated result of $P_{IN,avg}$ as a function of $t_{ON}$.

Fig. 4 shows the block diagram of the ZCS controller. It consists of a common-gate comparator to compare between $V_{ind}$ and ground, $M_{N2}$ for inducing $V_{ind}$ into the comparator, and several logic gates. The ZCS controller is operated when $\Phi_{P,LV}$ is rising edge. Once $\Phi_{P,LV}$ becomes high, $\Phi_N$ is high to connect $V_{ind}$ and comparator through $M_{N2}$. Even though the comparator always operates, it consumes power when $M_{N2}$ is turned on. Therefore, the ZCS controller consumes only 160 nW. Fig. 5 shows the simulated waveform of the ZCS controller. The delay prevents the shoot-through current, generating a short circuit when $M_P$ and $M_N$ are turned on simultaneously.

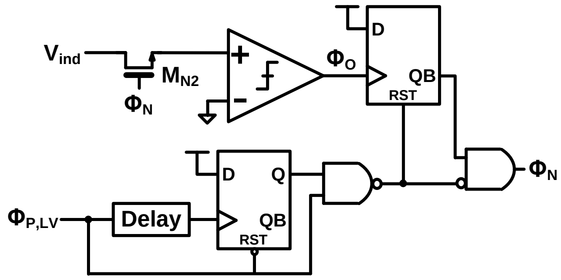

Fig. 4. The block diagram of the ZCS controller.

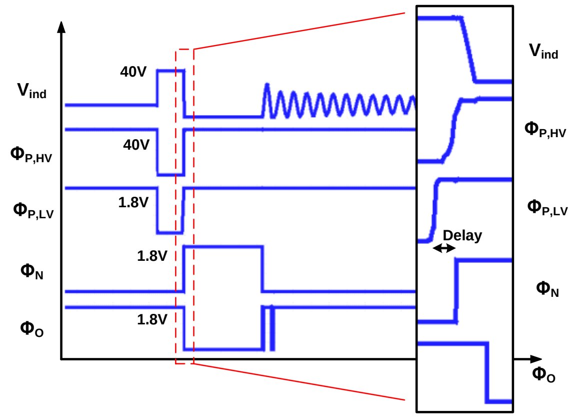

Fig. 5. Simulated waveform of ZCS controller in steady state.

## III. Experiment Result

The converter IC has been fabricated on a 180-nm BCD process. Fig. 6 shows the chip micrograph with an area of 3.055 mm$^2$. Table I shows a performance comparison with the state of the arts. All designs are fabricated using the BCD process supporting high voltage. Each process has its limit voltage: works [5],[6], and [8] have 70 V, work [7] has 60 V, and our work has 40 V. However, the maximum input voltage of works [5],[6], and [7] are saturated up to their limit voltage. On the other hand, work [8] and our work achieve harvest above the limit voltage. Even though work [8] makes the power possible to extract almost two times the limit voltage, it uses a multi-chip stacking technique, which increases the system's volume. Lastly, our work obtains 89.7 % conversion efficiency at output power ($P_{OUT}$) = 1.25 mW, comparable to the result of [8], which shows 70.7 % conversion efficiency when the $P_{OUT}$ delivers 1.2 mW.

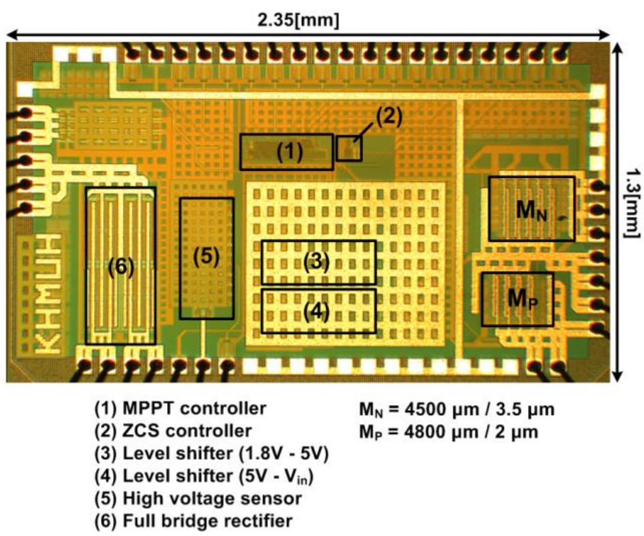

Fig. 6. Micrograph of the fabricated IC

TABLE I. PERFORMANCE COMPARISON

| | [5] | [6] | [7] | [8] | This work |
|---|---|---|---|---|---|
| Process | 180 nm HV BCD | 180 nm HV BCD | 250 nm HV BCD | 180 nm HV BCD | 180 nm HV BCD |
| Energy source | TENG | TENG | TENG | TENG | TENG |
| Type | Rectifier, Buck,[1]SC | Rectifier, Buck | Rectifier, Buck | [2]MCS-BF | Rectifier,Buck |
| MPPT technique | p-SSHI | FOCV | 2-D MPPT | - | Adaptive PWM |
| Inductor | 1 mH | 1 mH | 10 mH | 10 mH | 20 mH |
| $V_{OUT}$ | 2 V | 2 - 5 V | 0 - 5 V | 3.1 - 4.3 V | 2 - 5 V |
| $\eta_{CONV}$ | 32.71% @ $P_{OUT}$ = 722 μW | 54.48% @ $P_{OUT}$ = 20.7 μW | 85% @ $P_{OUT}$ = N/A | 70.7% @ $P_{OUT}$ = 1.2 mW | 89.7% @ $P_{OUT}$ = 1.25 mW |
| Area | 6.25 $mm^2$ | 2.482 $mm^2$ | 3 $mm^2$ | N/A | 3.055 $mm^2$ |
| Limit Voltage | 70 V | 70 V | 60 V | 70 V | 40 V |
| Maximum Input Voltage | 70 V | 70 V | 60 V | > 135 V | > 40 V |

[1]SC : Switched Capacitor [2]MCS-BF : Multi-Chip-Stacked Bias-Flip

## IV. CONCLUSION

A rectifier (FBR) is required to shape AC voltage from the input source (TENG) to realize the proposed model. The converter IC is implemented using a 180-nm HV BCD process in an area of 3.055 $mm^2$. The process has a limit voltage of 40 V, which is the breakdown voltage of high-voltage transistors. To avoid power loss from sampling, the converter uses adaptive pulse width modulation (PWM), increasing harvested input power. In addition, we use a Zener-diode array to clip the voltage to protect devices and to harvest more power above 40 V of input voltage. In measurement, a peak conversion efficiency of 89.7 % is achieved for delivering an output power of 1.25 mW.

## ACKNOWLEDGMENT

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