2023 International Research Conference of Sri Lanka Technology Campus
Colombo, Sri Lanka. 14th-15th December 2023

High-Efficiency Buck DC-DC Converter Using Automatic PWM/PFM Mode Control Based on Load Current Variation with Digital Soft Start

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***Abstract*—This paper proposes a dual-mode buck DC-DC converter that operates alternately between Pulse Width Modulation (PWM) and Pulse Frequency Modulation (PFM) modes, achieving high efficiency over a wide load range, making it suitable for applications in the Internet of Things (IoT) and biomedical technology fields. The zero-current detector (ZCD) technique is utilized for the purpose of eliminating negative current when the inductor is in a discontinuous conduction mode (DCM) state. It simultaneously transitions the converter into pulse frequency modulation (PFM) mode to reduce power losses under light load conditions. The converter utilizes current sensing to detect the inductor current in continuous conduction mode (CCM) and switches operation to PWM mode, achieving peak efficiency under high load currents. To ensure a precise and stable operation with fast response during operation this paper proposes a rail-to-rail comparator with wide bandwidth, combined with an efficient soft-start technique. Special, during operation, to mitigate the phenomenon of shoot-through caused by PMOS and NMOS at high frequencies, dead-time techniques are applied to avoid this issue. The converter is designed using 180 nm CMOS technology and achieves a peak efficiency of 96% with VDD = 3.3 V (standard battery voltage) and V_{OUT} ranging from 1.2 - 1.8 V. The load current advantageously spans from 250 - 3.5 mA, with load values ranging from 5 - 400 Ω. The switching frequency varies from 1.1 - 0.05 MHz, and the time for output voltage recovery between the two modes is 10 and 8 μs when transitioning from heavy to light load and vice versa.**

***Keywords*—DC-DC converter, on-chip, discontinuous conduction mode, continuous conduction mode.**

I. INTRODUCTION

The increasing demand for power management integrated circuits (ICs) is driven by the growing popularity of portable electronic devices. These ICs, especially buck DC-DC converters, play a crucial role in converting battery supplies into regulated voltages, supporting the advancement of battery- powered portable applications. [1-3]. High-efficiency buck DC-DC converters with a wide load current range are required to increase battery life. In reality, the pulse width modulation (PWM) scheme has high efficiency in heavy load because conduction loss, switching loss, and quiescent loss are relatively smaller than output power, whereas the pulse frequency modulation (PFM) scheme has high efficiency in light load because quiescent loss and switching loss are reduced by reducing switching frequency and selecting a small switch transistor size [4]. As a result, the study of PWM, and PFM dual-mode buck converters has long been a hotspot [5-7]. The PWM/PFM double buck converter is often made of a PWM modulation and a PFM modulator, which adds to the circuit's complexity [8]. Moreover, in PFM mode, the error amplifier is often switched off to decrease power dissipation and hence improve efficiency. As a result of the extended settling time of the error amplifier, the undershoot voltage is significant and the recovery time is protracted when the converter switches from PFM to PWM mode.

The Power Management Integrated Circuits (PMICs) are essential components that need to operate with high efficiency while consuming minimal energy. In battery-powered devices, battery replacement is often impractical, therefore optimizing power usage and load current is crucial to extend battery life. Because, there is a growing need for adaptive voltage converters capable of operating in both PWM (Pulse Width Modulation) and PFM (Pulse Frequency Modulation) modes, switching automatically based on the load conditions. These modes operate differently depending on load variations. In high-load conditions, as shown in Fig. 1(a), the converter operates in Continuous Conduction Mode (CCM) is inductor current never goes to zero during the switching cycle and continuously charged and discharged at a very high frequency. This maintains a stable current in the inductor, controlled

by the PWM voltage control mode, this mode enables a fast response of the output voltage, and stability, minimizes power losses in the switch, and efficiently transfers energy from the input to the output, achieving maximum efficiency with heavy loads. In contrast, at light-load conditions, as depicted in Fig. 1(b), the converter operates in Discontinuous Conduction Mode (DCM) using PFM control, this inductor current becomes discontinuous, meaning there are moments during the switching cycle when the current I_L drops to zero before the cycle ends. In mode PFM control, the switching frequency is adjusted based on the load, when the load is light switching frequency is lowered to reduce power losses in the inductor and switch, improving efficiency at light loads. However, in this mode, it is less stable compared to heavy load conditions.

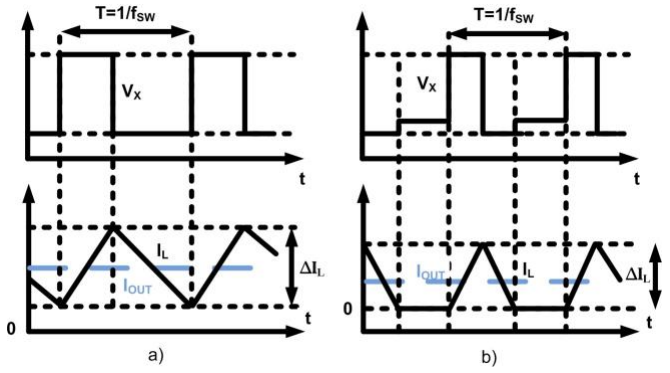

Fig. 1. (a) Inductor current of the DC-DC converter in mode CCM and (b) mode DCM operations

By combining both PWM and PFM control modes, a voltage converter can leverage the strengths of each mode and mitigate their weaknesses. This versatility allows the converter to adapt to varying load conditions effectively. Therefore, selecting the appropriate mode based on the specific load requirements is crucial for optimal performance. Such adaptive voltage converters play a vital role in extending the lifespan of battery-powered devices and optimizing their energy usage, making them a valuable solution in various applications.

II. Structure Buck Dc-Dc Converter with Pwm/Pfm Control Technology Combine with Soft Start

The buck converter averages the input voltage to produce a rectified output voltage. The buck converter in CMOS technology is similar but requires high accuracy, fast speed, high conversion efficiency, and a small chip area to meet applications in biomedical engineering. It works thanks to the switching frequency and the dominant characteristic of the inductor, from an input voltage through the buck converter, the output voltage is reduced. The output voltage will be changed when switching ON/OFF states S1/S2, adjusting the on/off time of switch S1/S2 causes the average output voltage to change according to the TON/TOFF cycle of S1/S2. When switch S1 is ON and S2 is OFF, current enters the inductor, the magnetic field in the inductor increases, the current in the inductor is negative, so the energy in the inductor is high, and the output voltage is low. When S1 is OFF, S2 is on, providing a ground current path, and the direction of current in the positive inductor supplying current to the output voltage load is increased. The two processes operate continuously, the output voltage of the converter is the average voltage of the two on-and-off processes S1/S2 over time. The output voltage is stable and can be adjusted within a certain limit. This paper implements a feedback control system for the on-off switching cycle of the switch.

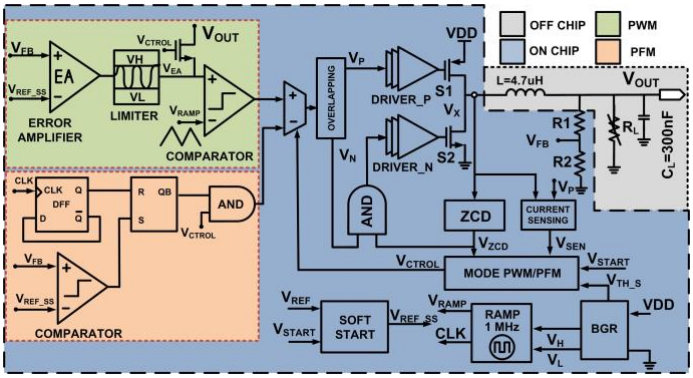

Fig. 2. Structure buck DC-DC converter using PWM/PFM control combined with soft start.

Fig. 2 depicts a buck DC-DC converter with PWM/PFM control and soft start. The PWM modulator and PFM modulator are combined using MUX to control the buck converter in either PWM or PFM mode. MUX is controlled by the V_{CTROL} signal to switch between the two modes, with logic '0' representing PWM mode and logic '1' representing PFM mode. The buck converter performs automatic mode switching based on the signal V_{CTROL}, which is set by a load current sensor. The V_{CTROL} has a state logic '0' when the load is light and '1' when the load becomes heavy.

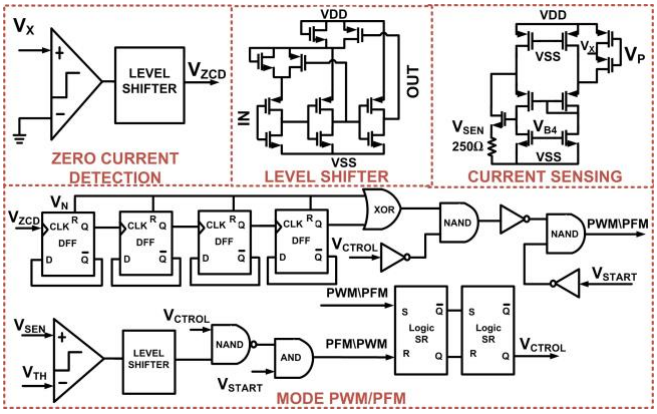

Fig. 3. The architecture of mode control PWM/PFM

Fig. 3 shows the PWM/PFM control block mode conversion block which detects the output current of the converter and

switches between PWM and PFM modes as necessary to optimize efficiency and performance. This helps to ensure that the converter operates in the most efficient mode based on the load conditions. This block is responsible for detecting the output current of the converter and includes detectors for PWM-to- PFM and PFM-to-PWM modes. The switch frequency is 1 MHz in PWM mode and 50 kHz in PFM mode. The Zero Current Detection (ZCD) block functions to detect the negative current I_L flowing in comparison to ground 0 V when S2 is open. If the output load is high, the output current will be low, and I_L will operate in DCM (Discontinuous Conduction Mode). At this point, the V_{ZCD} signal affects S2, preventing I_L from discharging into the negative current, and the current in the output capacitor is discharged only through the load. The signal comparing V_X to ground is passed through a LEVEL SHIFTER block to generate the V_{ZCD} signal with a high level, controlling the transition from PWM mode to PFM mode of the Buck DC-DC converter. The current sensing block is designed to detect fluctuations in the current at V_X, which is generated by the resistance of S1. The V_{SEN} signal increases and decreases in response to changes in the input current. The accuracy of V_{SEN} and the performance of the comparator circuit are crucial for the precise operation of the conversion system. The system switches from PFM mode to PWM mode based on the value of V_{SEN}.

The switching time between the two modes must differ by a 10μs interval, denoted as T_{ns} showed in Fig. 4 because the two modes switch at different load current values to prevent misinterpretation and continuous mode switching. The signal transitioning from high to low signifies a transition from PWM mode to PFM mode, whereas the signal transitioning from low to high indicates a shift from PFM mode to PWM mode. The PWM/PFM mode block operates quite accurately within a load current range spanning from 250 - 3.5 mA.

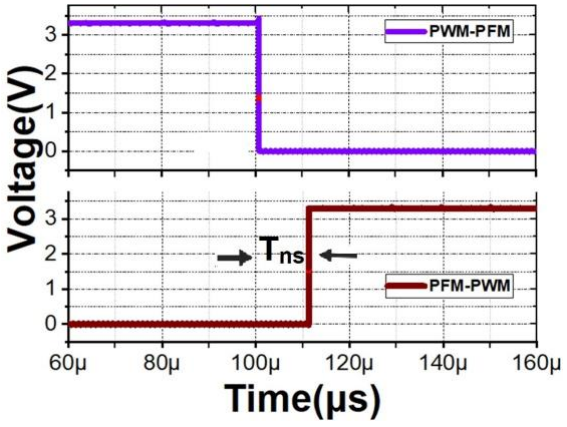

Fig. 4. The simulation waveforms of the proposed mode control PWM/PFM

The error amplifier consists of an error amplifier block along with a capacitor multiplier block, as shown in Fig. 5(a). The output voltage is fed back to the feedback block, where the feedback voltage V_{FB} is compared to the reference voltage

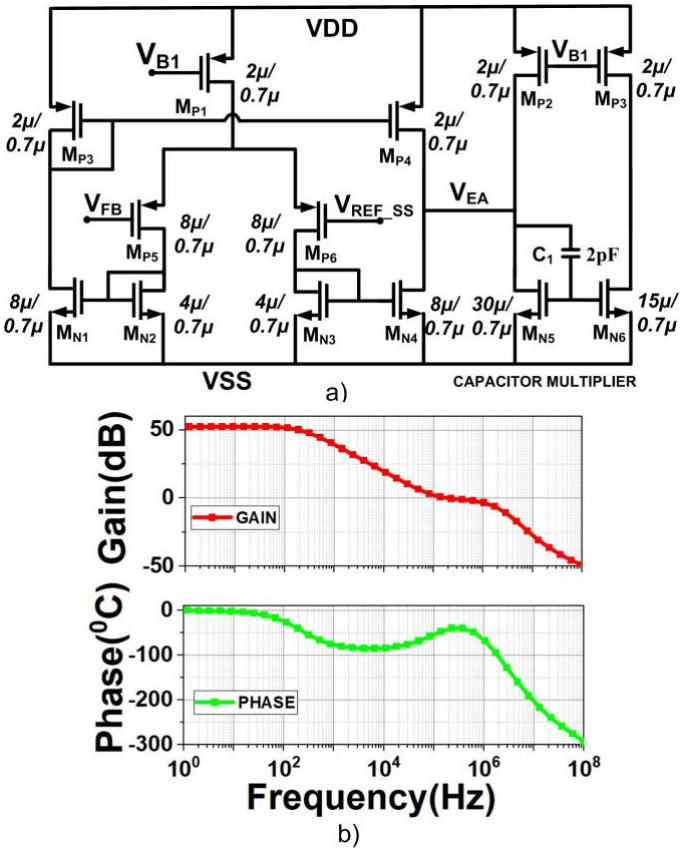

Fig. 5. (a) The architecture of error amplifier, (b) simulation gain phase

V_{REF_SS} through the error amplifier. The output voltage V_{EA} changes in response to V_{FB}, with a faster response due to the amplification factor. When V_{FB} decreases, V_{EA} decreases, and vice versa. The Operational Transconductance Amplifier (OTA) structure of the error amplifier operates with a gain of 50 dB and low power consumption to ensure the output signal. The application of the capacitor multiplier is to establish the static working point for stabilizing the V_{EA} signal while reducing the size of the capacitor. The VB1 points provide a reference voltage to create a current source for the circuit. Similar to a Type II Compensator, the capacitor multiplier uses an OTA to ensure the stable operation of the error amplifier, controlling the current flowing into the capacitor to maintain the stability of the V_{EA} signal without requiring a large capacitor size. The total circuit current consumption is 2 µA, supplied with a voltage of 3.3 V, and the power consumption of the error amplifier circuit is 6.6 µW. Fig. 5(b) illustrates the gain and phase characteristics of the error amplifier.

The architecture limiter V_{EA} showed in Fig. 6(a), includes two OTA comparison circuits connected together with V_{EA} limited by V_H and V_L, which are the upper and lower thresholds of the V_{RAMP} triangular wave. During start-up and mode switching, the V_{EA} circuit changes if it reaches V_H. At that time, M_{P10} is turned on, causing the V_{EA} voltage to drop below V_H, and then M_{P10} is turned off again capacitor C_3 ensures the

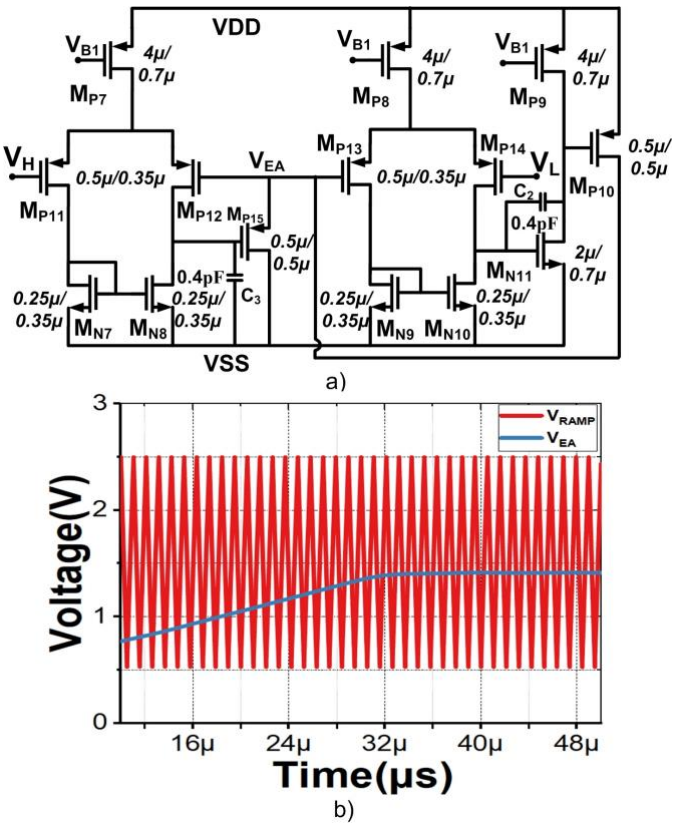

Fig. 6. (a) The architecture of limiter, (b) simulation limiter signal V_{EA}.

opening and closing process of M_{P10} is smooth, and V_{EA} does not exceed V_H. Conversely, if V_{EA} drops below V_L, M_{P15} is turned on, pulling the V_{EA} voltage up to a level greater than V_H and not dropping below the V_L threshold. Since V_L is a low voltage, an additional stage is needed, combined with capacitor C_2, to stabilize the opening and closing of M_{P15}. The V_{EA} limiting block ensures that the converter always stabilizes the V_{EA} signal within the limits of the triangular wave as shown in Fig. 6(b), creating the switching cycle of switches S1 and S2. Without the limiting block, the capacitor generating V_{RAMP} would have to be large, which could affect the size of the chip. Moreover, when the triangular wave limit is smaller, the rate of change of V_{EA} will increase, and the switching frequency cycle of the switch will change rapidly. This will significantly improve the stability time of V_{OUT} during operation or during load changes.

Fig. 7 shows the proposed architecture comparator rail to rail, the comparator is an essential component in a buck converter circuit. The accuracy of the comparator affects the conversion efficiency of the circuit. The conventional comparator consists of a PMOS or NMOS differential pair with low accuracy and input range dependent on the Voltage threshold of the NMOS or PMOS. To improve the accuracy and increase the bandwidth of the comparator, this paper proposes a rail-to-rail comparator without a clock signal. The circuit has the advantage of reducing noise on the comparator, and the input

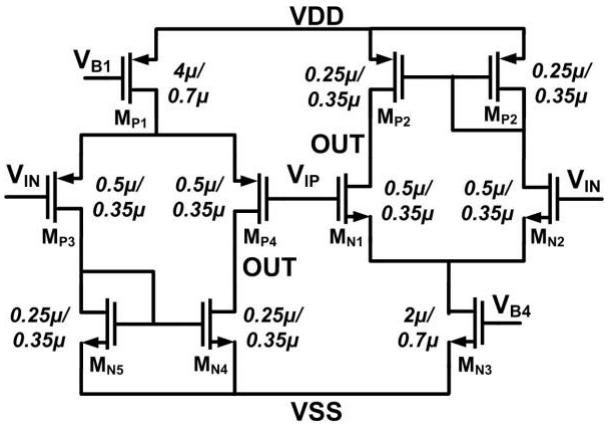

Fig. 7. The architecture of comparator rail to rail

range is not limited by the Voltage threshold of the PMOS or NMOS. This is because the input signal is applied to both

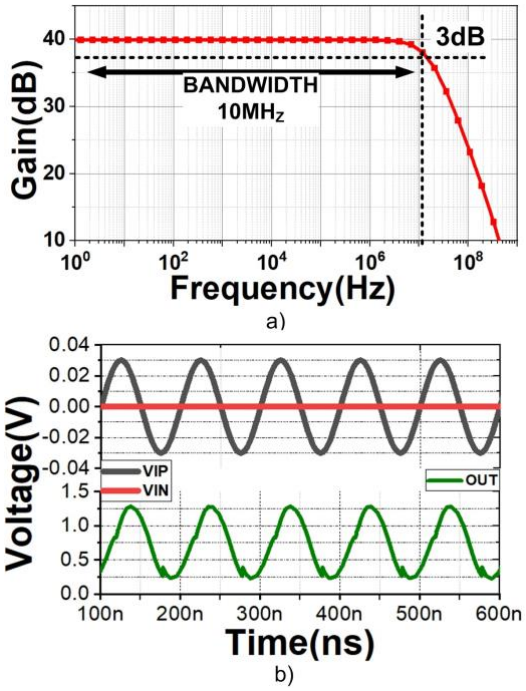

Fig. 8. (a) The simulation waveforms of bandwidth and (b) signal output comparator.

PMOS and NMOS at the same time, which can overcome this limitation. Additionally, the circuit can be compared at a frequency of less than 10 MHz based on bandwidth frequency Fig. 8(a), giving a sine wave signal with a frequency of 10 MHz amplitude of 25 mV to obtain an output signal in Fig. 8(b). In addition, the comparison speed of the circuit also depends on the current flowing through M_{P1} and M_{N3}. The larger the current, the faster the comparison speed. Fig. 9 shows the architecture of the soft start circuit which has an important role in smart electronic devices, especially in biomedical technology where startup circuits require high

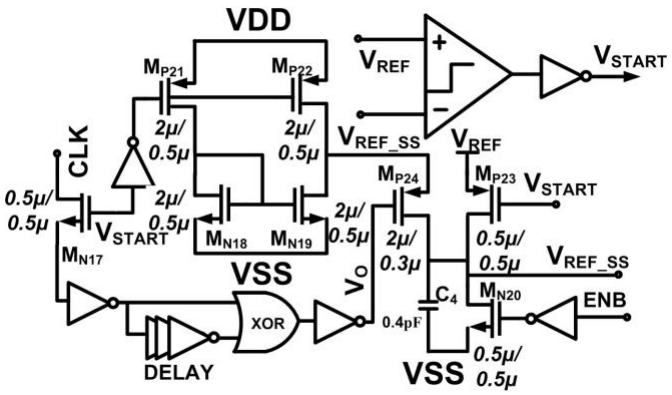

Fig. 9. The architecture of soft start

stability and precision. This paper proposes a simple control technique utilizing charging current and the time it takes to charge a capacitor to determine the startup time of the DC-DC converter. The charging time of the capacitor depends on the current flowing through M_{P24} into the capacitor for each CLK pulse delay. After the V_{REF_SS} voltage increases from 0 V to the desired reference voltage V_{REF} via the signal comparator V_C the CLK pulse is disabled by M_{N17}, and the charging current into the capacitor is cut off by M_{P21} and M_{P22}, while the V_{REF_SS} voltage is maintained at the V_{REF} voltage, as shown in Fig 10.

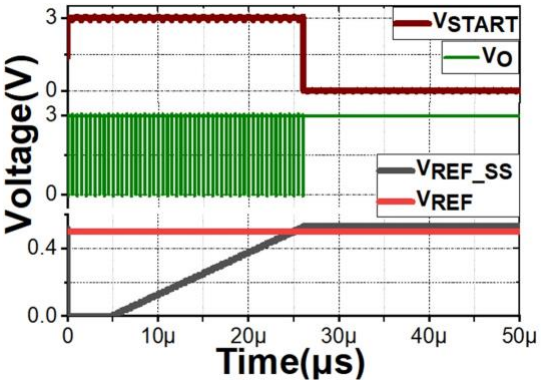

Fig. 10. The simulation waveforms of block soft start

The non-overlapping block serves to create a delay in the control pulses S1 and S2 in a switch. It utilizes the state of cross-connected NAND logic gates, as shown in Fig. 11(a) when one input of the NAND gate is driven to a logic '0', the output always transitions with a rising edge for V_N slower than V_P and with a falling edge for V_N faster than V_P. The remaining NOT gates are used to smooth the signals while increasing the slope for both V_N and V_P. Fig. 11(b) shows the delay time between V_N and V_P during the ON and OFF cycles is designed to prevent S1 and S2 from turning on simultaneously, which could lead to a high voltage touching ground and causing a short-circuit phenomenon. Fig. 12(a), shows the architecture proposed ramp generator circuit, this is a circuit used for

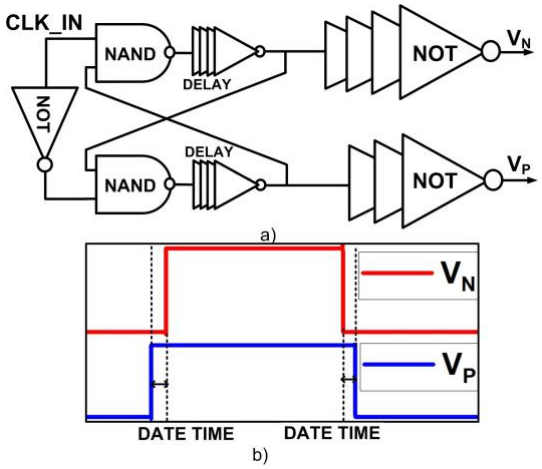

Fig. 11. (a) The architecture of block overlapping; (b) simulation signal V_N and V_P.

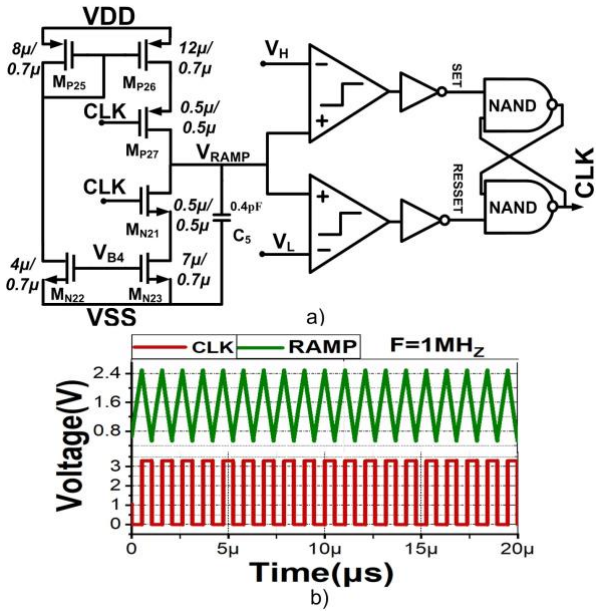

Fig. 12. (a) The architecture of block ramp generator and (b) simulation signal results.

generating a fixed-frequency triangle wave modulation, V_{RAMP} compared to V_{EA} for PWM wave modulation. Additionally, it generates the CLK signal to control soft-start blocks and PFM wave modulation. The V_{RAMP} voltage is created based on the charging and discharging principle of capacitor C_5, which produces a pulse waveform input to the comparator with low voltage V_L and high voltage V_H. During the charging or discharging process, the pulse waveform reaches V_H or V_L, creating SET and RESET signals on the SR latch logic and generating the CLK signal as shown in Fig 12 (b). Fig. 13(a) shows this paper proposes architecture bandgap reference using generates a stable voltage regardless of temperature. The CMOS transistors M_{P31}, M_{P32}, M_{N24}, M_{N25} have the same gate voltage initially. As temperature rises, current through the

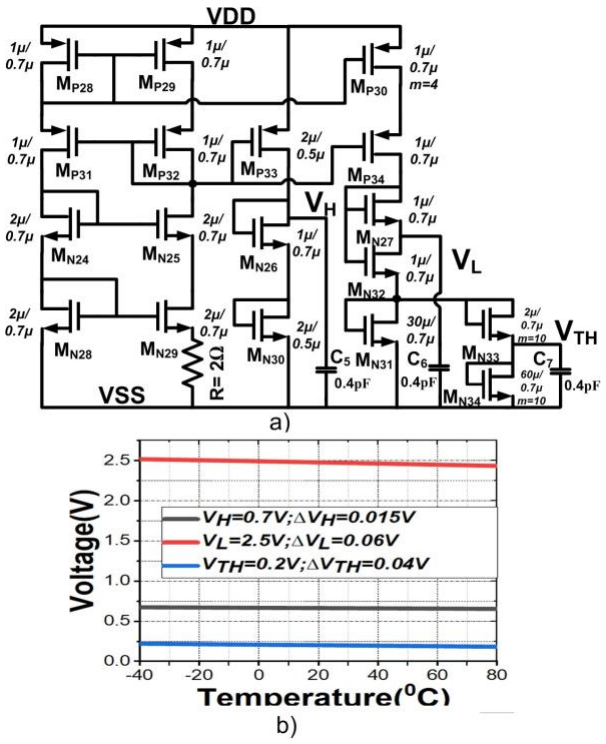

Fig. 13. *(a)* The architecture of block bandgap reference and (b) simulation signal results.

CMOS devices increases, changing the gate voltage values. An increase in gate voltage results in an increase in the resistance of M_{P31} and M_{P32}, while decreasing the resistance of M_{N24} and M_{N25}. The gate voltage will thus vary according to the temperature fluctuation. Fig 13(b) shows points V_H, V_L, and V_{TH} are maintained within a certain temperature range.

III. Results and Discussion

This paper proposes a design dual-mode PWM/PFM buck DC-DC converter implemented in 180nm CMOS technology. The chip layout occupies a compact area of 0.067 mm², as illustrated in Fig. 14. The converter operates in two distinct modes PWM and PFM based on load conditions, providing enhanced efficiency with a peak performance of up to 96%. Additionally, it integrates a soft start block as shown in Fig.9, with a startup time of approximately 25 μs to ensure stability and mitigate noise caused by V_{REF}. The simulation results of load variations in dual mode PWM/PFM buck DC-DC converters are displayed in Fig. 15. The transition between PWM and PFM modes is controlled by the V_{CTROL} signal, with the load current I_L switching from Continuous Conduction Mode (CCM) corresponding to 5 Ω load to Discontinuous Conduction Mode (DCM) corresponding to a 400 Ω load, as shown in Fig. 15(a). Conversely, the transition from PFM to PWM mode is controlled by the V_{CTROL} signal in the opposite direction, switching from PWM to PFM in shown Fig. 15(b). It is noteworthy that in the PWM mode, the converter is considered to be in a sleep state, and the output voltage is

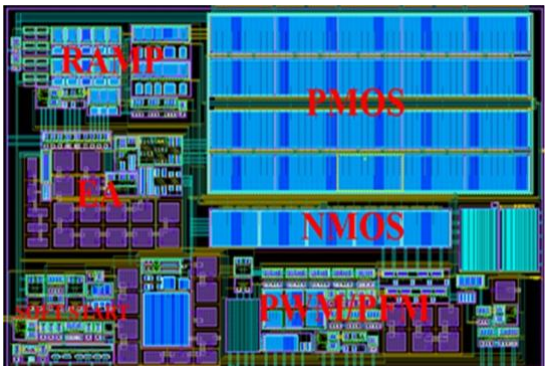

Fig. 14. *The buck converter layout results*

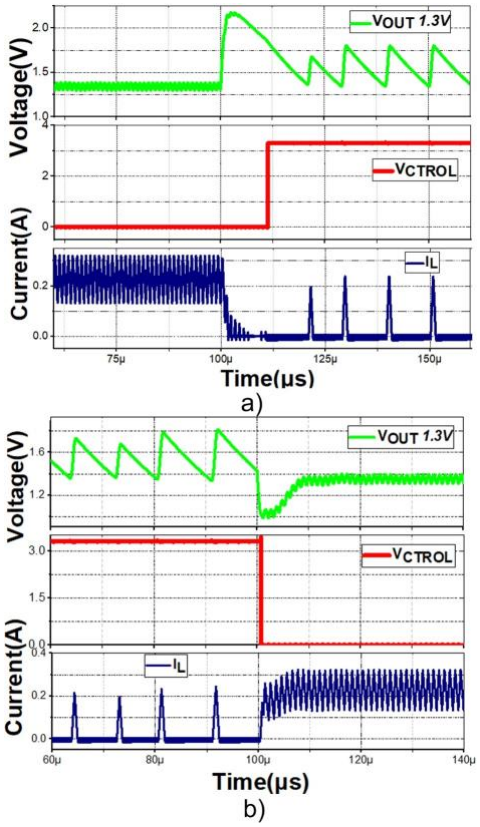

Fig. 15. *(a)* The simulation waveform model switching mode PWM-PFM and (b) PFM-PFM.

unstable compared to the PWM mode where the chip operates at high efficiency.

Fig. 16 depicts the variation in the output current I_{OUT} and input current I_{OUT} as it transitions from a heavy-load mode to a light-load mode have I_{OUT} decreases from 230 to 3.5 mA. By examining the input and output currents, we can calculate the conversion efficiency of the Buck DC-DC converter in shows Fig. 17, allowing us to assess its operational effectiveness. The load resistance R_L will correspondingly change, depending on the voltage values present on it, as shown in Fig. 18. To set the output voltage to different levels within the range of 1.2-1.8 V, switches SW1, SW2, and SW3 are sequentially

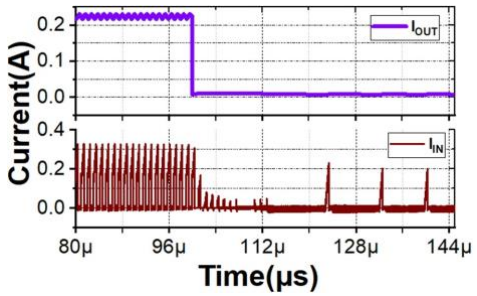

Fig. 16. The simulation current DC-DC buck converter.

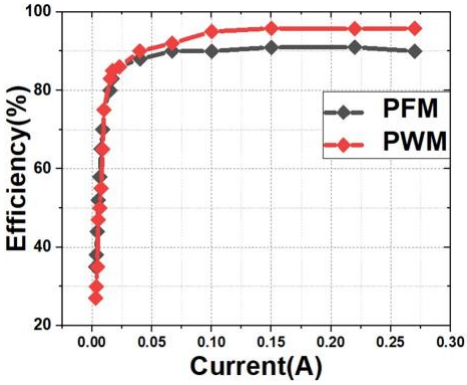

Fig. 17. The efficiently switching mode PFM/PWM.

turned on to adjust the corresponding V_{REF} reference values, as depicted in Fig. 19. The input voltage passes through different resistor networks with varying resistance values, resulting in different V_{REF} values that control the output voltage V_{OUT}. The external circuitry ensures stable operation and chip protection. Performance comparisons with other research are presented in Tab. 1.

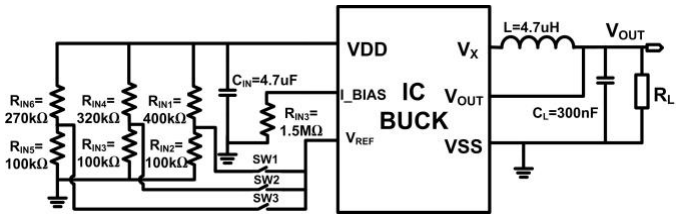

Fig. 18. The diagram of the connection outside the chip of the Buck - DC converter.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON.

Architecture	[9]	[10]	[11]	**This work**
Technology(um)	0.4	0.18	0.35	0.18
Control Loop	PWM	PWM	PWM/PFM	PWM/PFM
Frequency (MHz)	1	0.7	N/A	1/0.05
Input Supply (V)	5	3.3	3.6	3.3
Output Voltage (V)	1.8	2.4	1.8	1.2-1.8
Max Load Current (A)	1	0.25	0.5	0.18
Peak Efficiency (%)	91	94	88	96
Overshoot voltage recovery time (µs)	27	12	28	10
Undershoot voltage recovery time (µs)	31	12	10	8

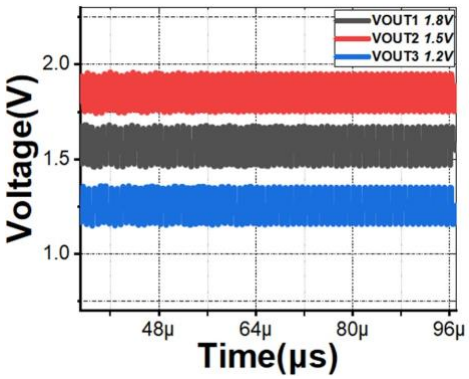

Fig. 19. The simulation output voltage waveform shape in mode PWM.

IV. CONCLUSION

This paper presents a PWM/PFM control technique to improve the output load current variation, combined with a soft-start technique for stable startup of the buck DC-DC converter system, applied in handheld smart electronic devices and biomedical technology. Switching between the two modes of PWM/PFM improves the conversion efficiency over the load variation range. The load efficiency is significantly improved when operating in PFM mode, which helps the converter consume less energy. Simulation results demonstrate that the proposed PWM/PFM control technique can perform automatic mode switching between PWM and PFM modes during the conversion process combined with the soft-start block, the system achieves stable startup.

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